IDEC Chip Design Contest

A Resolution-Reconfigurable SAR ADC with compensation for PVT variations

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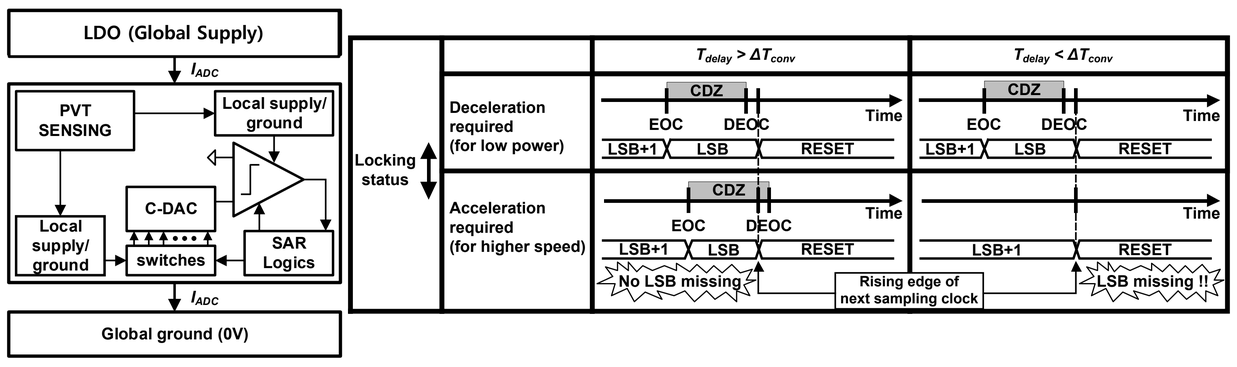
Introduction

The successive approximation register (SAR) analog-to-digital converters (ADCs) are the most promising candidate for low power applications such as battery-powered sensor nodes and bio-medical systems. In order to increase power efficiency, SAR ADCs operating at low supply voltage have been reported. Since the lowered supply voltage can cause many problems such as leakage current, low signal-to-noise ratio (SNR), and vulnerable performance to process, voltage and temperature (PVT) variations, many studies for low supply SAR ADC have been conducted. However, the previous researches mostly focus on the effects of leakage or low SNR, where fabricated MOS transistors using with low supply voltage inevitably also suffer from the performance instability due to PVT variations. If the uncertainty of PVT variations is considered, ADCs should have much faster conversion speed than target specification. But unnecessary power is consumed under PVT conditions that cause large current.

To emphasize the influence by PVT variations on the performance of low supply voltage circuits, a conversion time of ADC has been simulated at the variety of PVT conditions. The proposed system detects the PVT variation by monitoring the conversion speed and then controls the supply voltage to compensate the performance degradation by PVT in real time. The conversion time is shorted by the increase in supply voltage to compensate the PVT variations. However, in case of the other PVT conditions, the supply voltage level is lowered again to retain low power operation without the performance degradation.

PVT compensation techniques



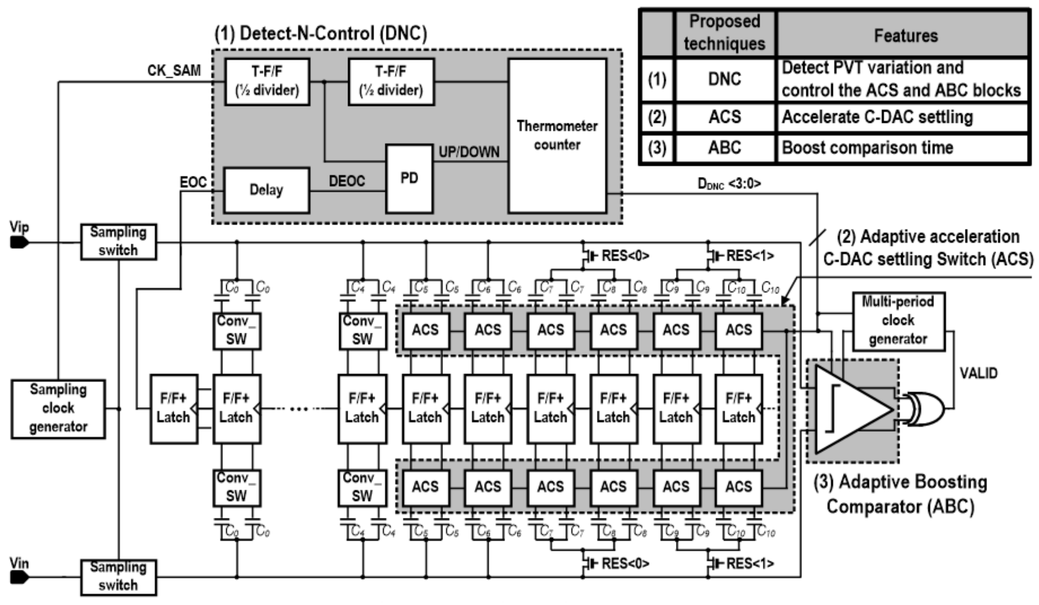
(a) (b)

Figure 1. (a) The conceptual block diagram of proposed PVT compensation; (b) Criteria to prevent LSB missing in locking state

Fig. 1. (a) shows the conceptual block diagram of the proposed PVT compensation system. Assuming LDO supports the ADC's global supply voltage and the current is represented by I_{ADC}. Once the 'PVT SENSING' block gives the information of PVT to the 'local supply/ground' blocks, VDD and VSS voltages are adjusted to multi-levels for comparator and switches of 'C-DAC'. In the feedback loop of the SAR ADC, the comparison time of comparator and settling time of 'C-DAC' are the bottlenecks for the overall conversion speed. Moreover, this problem becomes worse when resolution of ADC is increased. Thus, the changes in supply/ground voltages for these blocks can control the conversion speed of ADC. Also, from the LDO point of view, since the power consumed by the overall system is changed due to the variations in I_{ADC} by PVT conditions, the proposed architecture assures the reconfigurable low-power performance. The PVT variation should be sensed with the following criteria.

$$T_{conv} + T_{delay} > T_{target}$$
$$T_{delay} > |\Delta T_{conv}|$$

where T_{conv} and T_{target} are the time to compare the all bits and target conversion time. According to the detection result, thermometer based digital code (D_{DNC}) is increased or decreased to provide the information about PVT variation. Then, the conversion speed of SAR ADC is accelerated or decelerated according to the D_{DNC}. After several sequences of tracking the PVT, acceleration and deceleration are repeated with two D_{DNC}, which is so called locking state. Because the PVT variation is detected in real time, the D_{DNC} values are changed according to the PVT conditions. Then, the conversion speed and local supply/ground are also adjusted for low power



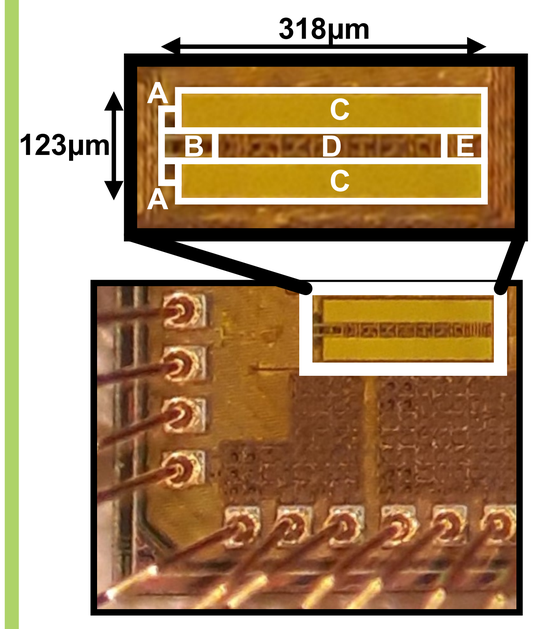
	Proposed techniques	Features
(1)	DNC	Detect PVT variation and control the ACS and ABC blocks
(2)	ACS	Accelerate C-DAC settling
(3)	ABC	Boost comparison time

Figure 2. Block diagram of proposed SAR ADC.

Then, the conversion speed and local supply/ground are also adjusted for low power consumption without accuracy degradation.

To support multi-level VDD and VSS for sub-blocks, only temporal voltage shift is needed because all sub-blocks of SAR ADC are the dynamic circuits. If VDD and VSS voltages are shifted by capacitors before operating, the sub-blocks operate faster with high $|V_{GS}|$. Once the operation is completed, the capacitors are charged again during reset phase. Since there is a trade-off between the highest $|V_{GS}|$ and charge for capacitor, more power consumption is required for wider PVT variation coverage. However, the proposed architecture uses an adaptive control and thus the required extra power is adjusted according to PVT variations, resulting in the improved efficiency.

Measurement Results



Area	Name
A	Sampling switches
B	ABC
C	Capacitive DACs
D	SAR logics + ACSs
E	DNC

	This work		
Technology (nm)	65		
Supply voltage (V)	0.5		
Sampling rate (KSPS)	300		
Resolution (bit)	8	10	12
DNL (LSB)	0.11	0.27	0.79
INL (LSB)	0.11	0.27	1.41
SNDR (dB)	60.34		
Power (μm)	1.8		
FoMW(FJ/conv(μm-step)	7.06		
Area (mm^2)	0.039		

Figure 3. Die photo and measured result with different resolutions.

The dynamic performances of the proposed ADC are shown at the 8, 10, and 12bit modes. The performances of SNDR at low frequency (10kHz) are 47.63, 57.36, 62.33 dB, respectively. At near Nyquist frequency are 47.63, 54.58, and 58.11 dB, respectively. The performances of SFDR at low frequency (10kHz) are 38.82, 67.59, 70.25 dBc. Also, the performances of SFDR at near Nyquist frequency are 38.82, 62.83, and 70.66 dBc.

Acknowledgment

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